WHAT IS CLAIMED IS:

1. An input/output protection device for a semiconductor integrated circuit including a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, comprising:

a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite to the first conduction type and being connected to the input/output terminal;

a second diffusion layer of the second conduction type connected to the electrode wiring kept, the electrode wiring being at a predetermined potential; and

a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer,

the first diffusion layer being circularly enclosed with the third diffusion layers.

2. An input/output protection device in accordance with claim 1, wherein the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor substrate.

3. An input/output protection device in accordance with claim 2, wherein the impurity concentration of the fourth diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof.

4. An input/output protection device in accordance with claim 2~~-or 3~~, wherein the third diffusion layer has a depth equal to or

more than that of the fourth diffusion layer.

5. An input/output protection device in accordance with ~~one of claims 1 to 4~~ claim 1, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

6. An input/output protection device in accordance with ~~one of claims 1 to 5~~ claim 1, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

7. An input/output protection device in accordance with ~~one of claims 1 to 5~~ claim 1, wherein the first and second diffusion layers are manufactured with a gate electrode disposed on a surface of the semiconductor substrate.

8. An input/output protection device in accordance with ~~one of claim 6 or 7~~ claim 6, wherein the device separating isolation layer or the gate electrode is fabricated in a circular shape.

9. An input/output protection device in accordance with ~~one of claim 7 or 8~~ claim 7, wherein the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor integrated circuit.

10. An input/output protection device in accordance with ~~one of claim 7 or 8~~ Claim 7, wherein the gate electrode is fixed to a predetermined potential.

11. An input/output protection device in accordance with claim 1 ~~one of claims 1 to 10~~, wherein:

the first conduction type is a p type and the second conduction type is an n type; and

the predetermined potential is a ground potential.

12. An input/output protection device in accordance with claim 1 ~~one of claims 1 to 10~~, wherein:

the first conduction type is an n type and the second conduction type is a p type; and

the predetermined potential is a potential of a power source.

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